

MEMORY ADDRESS SPACE EXTENSION DEVICE AND STORAGE MEDIUM STORING THEREIN PROGRAM THEREOF

BACKGROUND OF THE INVENTION

The present invention relates to a memory address space extension device and a storage medium storing therein a program thereof in which the memory address space extension device converts a CPU
5 (central processing unit) address into an extended address and the program executes processing memory address space extension.

Description of the Prior Art

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A conventional memory address extension device includes a register bank in every task. The register bank consists of a plurality of
10 page registers which are combined therewith. The page register stores therein CPU (central processing unit) address and upward address of extended address which is broader than the CPU address. When task switch occurs, the memory address extension device extends memory address space in such a way of causing the register bank to be switched.

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15 However, in the conventional technique described above, on the supposition that there exists a data to which only certain task accesses. However, another task capable of accessing such the data to which only determined certain task should access. Therefore, there is the problem
20 that the data which should only be accessed by the determined certain task is capable of being rewritten wrongly by the another task.

SUMMARY OF THE INVENTION

In view of the foregoing, it is an object of the present invention, in order to overcome the above mentioned problem, to provide a memory
25 address space extension device and a storage medium storing therein a program thereof which enable rewrite data wrongly according to task to be prevented in order to protect the data.

It is another object of the present invention, to provide a memory address space extension device and a storage medium storing therein a program thereof enable the data to which only certain task should access to be prevented from accessing wrongly by interruption processing to such
5 the data in order to protect it.

According to a first aspect of the present invention, in order to achieve the above mentioned object, there is provided a memory address space extension device which comprises a definition table for defining an access right of a task ID (identification) with respect to a data area, a task
10 ID register for storing therein the task ID of a task during execution, an extraction means for extracting a data area ID from a CPU (central processing unit) address inputted previously, a judgement means for judging as to whether or not it is capable of being permitted that the task during execution indicated by the task ID accesses the data area
15 indicated by the data area ID while referring to the definition table from both of data area ID extracted previously and the task ID stored in the task ID register.

According to a second aspect of the present invention, in the first aspect, there is provided a memory address space extension device,
20 wherein there are provided an address operational means for converting the CPU address into an extended address, and a memory having the extended address converted previously, when the judgement means judges that judgement result according to the judgement means is a result that the task during execution accesses the data area, the address
25 operational means executes the conversion processing.

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According to a third aspect of the present invention, in the first aspect, there is provided a memory address space extension device, wherein, as to the definition table, it causes combination that access is permissible or in-permissible with respect to read and / or write to the
30 data area respectively to be defined.

According to a fourth aspect of the present invention, in the first aspect, there is provided a memory address space extension device, wherein there is provided a forming means for forming said definition table.

5 According to a fifth aspect of the present invention, there is provided a storage medium for storing therein a program in order to execute the processing of a storing processing for storing a task ID of a task during execution, an extraction processing for extracting a data area ID from a CPU address inputted previously, and a processing for judging
10 as to whether or not it is capable of being permitted that the task during execution indicated by the task ID accesses the data area indicated by the data area ID while referring to the definition table from both of data area ID extracted previously and the task ID stored in the task ID register.

 According to a sixth aspect of the present invention, in the fifth
15 aspect, there is provided a storage medium for storing therein a program, wherein the program executes the processing of an address operational processing for converting the CPU address into an extended address when judgement result according to the judgement processing is that the task is permitted that the task during execution accesses the data area.

20 According to a seventh aspect of the present invention, in the sixth aspect, there is provided a memory address space extension device which comprises a definition table for defining an access right of a task with respect to a data area, and an access right judgement means for judging whether or not it causes the access right to the data area which the task
25 requests to be given with respect to the task according to the definition table.

 According to an eighth aspect of the present invention, in the seventh aspect, there is provided a memory address space extension device, wherein the definition table defines as to whether or not the task
30 possesses an access right for accessing prescribed data area in every task

ID given to the task.

According to a ninth aspect of the present invention, in the seventh aspect, there is provided a memory address space extension device, wherein the definition table defines as to whether or not said task
5 possesses an access right for accessing prescribed data area in every task ID given to the task and / or in every interruption number given to interruption processing.

According to a tenth aspect of the present invention, in the seventh or eighth aspect, there is provided a memory address space extension
10 device, wherein the access right judgement means judges whether it causes the access right to the data area requested by the task to be given according to the task ID, and the data area ID indicating the data area requested by the task.

According to an eleventh aspect of the present invention, in the
15 seventh or ninth aspect, there is provided a memory address space extension device, wherein the access right judgement means judges whether it causes the access right to the data area requested by the task to be given according to any one of the task ID and the interruption processing number, and according to the data area ID indicating the data
20 area requested by the task.

According to a twelfth aspect of the present invention, in any one of the seventh to the eleventh aspects, there is provided a memory address space extension device, wherein the definition table defines whether or not it causes access to be permitted with respect to the
25 prescribed data area in every the task.

According to a thirteenth aspect of the present invention, in any one of the seventh to the eleventh aspects, there is provided a memory address space extension device, wherein the definition table defines any one of:

30 (1) causing only write of the data to be permitted;

- 5 with respect to the prescribed data area in every said task.

According to a fifteenth aspect of the invention, in any one of the ninth, the eleventh, the twelfth, the thirteenth, and the fourteenth aspects, there is provided a memory address space extension device, wherein there is further provided an interruption number decoding means for decoding an interruption number from an interruption instruction with respect to the interruption instruction according to software.

According to a seventeenth aspect of the present invention, in any one of the seventh to the sixteenth aspects, there is provided a memory address space extension device wherein there is further provided a

definition table forming means for forming the definition table.

According to an eighteenth aspect of the present invention, there is provided a storage medium storing therein a program in order to execute the processing of a definition table preparation processing for preparing a definition table, a reference processing for the sake of the definition table which defines an access right of a task with respect to data area, and an access right judgement processing for judging whether or not it causes the access right for the data area requested by a task to be given to the task according to the definition table.

According to a nineteenth aspect of the present invention, in the eighteenth aspect, there is provided a storage medium storing therein a program, wherein the reference processing for definition table is the reference processing that it causes the definition table defining whether or not the task possesses the access right for accessing prescribed data area to be seen in every task ID given to the task.

According to a twentieth aspect of the present invention, in the eighteenth aspect, there is provided a storage medium storing therein a program, wherein the reference processing for definition table is the reference processing that it causes the definition table defining whether or not the task possesses the access right for accessing prescribed data area to be seen in every task ID given to the task and / or in every interruption number given to the interruption processing.

According to a twenty-first aspect of the present invention, in the eighteenth or nineteenth aspects, there is provided a storage medium storing therein a program, wherein the access right judgement processing judges whether or not the task possesses the access right for accessing prescribed data area according to the task ID and / or the data area ID indicating the data area requested by the task.

According to a twenty-second aspect of the present invention, in the eighteenth or the twentieth aspect, there is provided a storage

medium storing therein a program, wherein the access right judgement processing judges whether or not the task possesses the access right for accessing prescribed data area according to any one of the task ID and the interruption processing number and / or the data area ID indicating the data area requested by the task.

According to a twenty-third aspect of the present invention, in any one of the eighteenth to the twenty-second aspects, there is provided a storage medium storing therein a program, wherein the reference processing for definition table is the reference processing that it causes the definition table defining whether or not the task possesses the access right for accessing prescribed data area to be seen in every the task.

According to a twenty-fourth aspect of the present invention, in any one of the eighteenth to the twenty-second aspects, there is provided a storage medium storing therein a program, wherein the program executes the reference processing for definition table, which is the reference processing that it causes any one of:

- (1) allowing only write of the data to be permitted;
- (2) allowing read of the data to be permitted;
- (3) allowing write of the data and read of the data to be permitted;

and

(4) allowing no-access to be permitted,
to be seen with respect to the prescribed data area in every the task.

According to a twenty-fifth aspect of the present invention, in any one of the twentieth, the twenty-second, the twenty-third, and the twenty-fourth aspects, there is provided a storage medium storing therein a program, wherein the program further executes interruption number generation processing for generating interruption number to interruption processing according to hardware.

According to a twenty-sixth aspect of the present invention, in any one of the twentieth, the twenty-second, the twenty-third, the twenty-

fourth, and twenty-fifth aspects, there is provided a storage medium storing therein a program, wherein the program further executes interruption number decoding processing for decoding interruption number from interruption instruction with respect to said interruption instruction according to software.

According to a twenty-seventh aspect of the present invention, in any one of the eighteenth to the twenty-sixth aspects, there is provided a storage medium storing therein a program, wherein the program executes an address operational processing in order to convert a CPU address into an extended address in such a way that the address operational processing causes the CPU address to be converted into the extended address when the task is judged that the task is permitted to access to the data area according to the access right judgement processing, before executing storage processing of the converted address into a memory.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with the accompanying drawings. It should be expressly understood, however, that the drawings are for purpose of illustration only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a first block diagram showing a configuration of a memory address space extension device in an embodiment of the present invention;

Fig. 2 is a block diagram showing a configuration of an address operational unit in the embodiment of the present invention;

Fig. 3 is a constitution view showing register bank selection table in the embodiment of the present invention;

Fig. 4 is a first data area access right definition table in the

embodiment of the present invention;

Fig. 5 is a constitution view in the case of forming execution form file from data class definition file in the embodiment of the present invention;

5 Fig. 6 is a second data area access right definition table in the embodiment of the present invention;

Fig. 7 is a second block diagram showing a configuration of the memory address space extension device in the embodiment of the present invention;

10 Fig. 8 is a third data area access right definition table in the embodiment of the present invention;

Fig. 9 is a fourth data area access right definition table in the embodiment of the present invention;

15 Fig. 10 is a flowchart explaining a first operation of the memory address space extension device in the embodiment of the present invention; and

Fig. 11 is a flowchart explaining a second operation of the memory address space extension device in the embodiment of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will be described in detail accompanying the drawings.

25 Fig. 1 is a block diagram showing a first embodiment of a memory address space extension device according to the present invention.

In Fig. 1, the memory address space extension device comprises a CPU1 having a certain address space, a memory 2 having extended address which is broader address space than that of the CPU1, and a memory management unit (hereinafter referred to as MMU) 3.

30 The MMU3 consists of a task ID register 4 storing therein the task

ID of a task with execution conditions, and an address operational unit 5 converting a CPU address into an extended address.

Fig. 2 is a constitution of the address operational unit 5 of Fig. 1.

In Fig. 2, the address operational unit 5 consists of a page register 7 for storing page register data necessary for calculating the extended address, a plurality of register banks 6 which are combined to be constituted by a plurality of the page registers 7, a register bank control unit 8 for obtaining register bank number from both of data area ID which is a part of the CPU address and task ID, and a cache 9.

The cache 9 accommodates both of a register bank selection table 10 as shown in Fig. 3 and a data area access right definition table 11 as shown in Fig. 4.

(FIRST OPERATION)

Next, there will be explained operation.

The address operational unit 5 inputs therein the CPU address from the CPU1. The CPU address consists of data area ID, register bank address, and offset address.

The address operational unit 5 decomposes the inputted CPU address into above data area ID, a register bank address, and an offset in order to extract thereof (STEP S102). Next, a register bank control unit 8 refers to the data area access right definition table 11 existing in the cache 9. The task ID is stored in the task ID register 4. It causes the access right for the data area to be requested to the task during execution from both of the task ID stored in the task ID register 4 and the data area ID which is extracted (STEP S103). When the access is not permitted (STEP S103/NO), the access is not executed to the data area, thus system error occurs (STEP S105).

When the access is permitted (STEP S103/YES), it causes the register bank number of the data area which is attempted to access to be obtained while referring to the register bank selection table 10 existing in

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the data area B to be not implemented, thus the system error occurs. While when the task whose task ID is 1 (one) attempted to rewrite the data existing in the data area A, since the access right of the data area access right definition table 11 of Fig. 6 is permissible, it causes the register bank number to be obtained while referring to the register bank selection table 10 existing in the cache 9.

Further, a storage unit such as ROM (read only memory) and so forth storing therein a program in a computer system constitutes the memory address space extension device of Fig. 1. Thus the storage unit of the ROM and so forth constitutes a storage medium according to the present invention. The storage medium stores therein the program indicating processing in order to execute operation described in the above respective embodiment.

It is capable of being used an optical disk, a magneto-optical disk, a magnetic recording medium, a semiconductor memory, and so forth as the storage medium.

(THIRD OPERATION)

Fig. 7 is a second block diagram showing constitution of the memory address space extension device in the embodiment of the present invention. The memory address space extension device shown in Fig. 7 comprises a CPU 71, a memory 72, a memory management unit (MMU) 73, and an interruption control unit (ICU) 76.

The CPU 71 possesses prescribed address space. The memory 72 possesses an extended address which is address space broader than address space which the CPU 71 possesses.

Further, the memory management unit (MMU) 73 consists of a task ID register 74, an address operational unit 75, and a decoder 77.

The task ID register 74 accommodates task ID of a task which is effective condition. The task ID register 74 accommodates an interruption number of interruption processing during execution too.

The address operational unit 75 converts the CPU address into the extended address. The interruption control unit (ICU) 76 produces interruption according to hardware.

Fig. 7 shows the memory address space extension device. Operation in which it causes the extended address to be obtained will be explained in detail referring to Figs. 2, 3, 5, 7, and 11. The extended address is obtained with respect to the task that is under the condition that access in relation to a certain data area is not permitted. The extended address is also obtained with respect to the task which is under the condition that access is permitted, while preventing wrong access according to interruption processing.

As shown in Fig. 5, on the inside of the memory address space extension device, the linker / locator forms the execution form file from among the object file, the data class in which a plurality of data is gathered, the data class definition file which defines the access right of such the data class (STEP S110). On this occasion, the data whose data class is identical therewith is arranged while collecting.

Fig. 8 is a third data area access right definition table in the embodiment of the present invention. As shown in Fig. 8, with respect to the present embodiment, on the supposition that the task of "101", "102", "103", and "104" exists as the task ID, the interruption processing of "1", "2", and "3" exists as the interruption number. Further, on the supposition that there exists "area A", "area B", and "area C" as the data area.

The interruption processing of the interruption numbers "1" and "2" is taken to be the interruption processing according to software. The interruption processing of the interruption number "3" is taken to be the interruption processing according to hardware.

The memory address space extension device shown in Fig. 7 forms the register bank selection table shown in Fig. 3 to the cache 11 on the

occasion of initialization. The memory address space extension device also forms the data area access right definition table shown in Fig. 8 to the cache 11 on the occasion of initialization (STEP S111).

When the system operates, OS (Operating System) accommodates
5 the task ID of the task which is under effective condition into the task ID register 74. When the task switch occurs, the OS accommodates the task ID which becomes effective condition according to the task switch into the task ID register 74.

The interruption according to hardware occurs during system
10 operation. On this occasion, the interruption control unit (ICU) 76 produces interruption number. The produced interruption number is accommodated in the task ID register.

The CPU 71 causes the interruption instruction according to the software to be executed. On this occasion, the interruption number
15 which is decoded by the decoder 77 is accommodated in the task ID register 74.

Furthermore, when the instruction for returning from the interruption processing is executed, the CPU 71 accommodates the task ID of the task which is in the effective condition immediately before
20 execution of the interruption processing into the task ID register 74.

The address operational unit 75 decomposes the CPU address inputted from the CPU 71 into the data area ID, the register bank address, and the offset (STEP S112).

The register bank control unit 8 in the address operational unit 75
25 refers to a data area access right definition table 81 shown in Fig. 8 accommodated the cache 11 according to the task ID stored in the task ID register, or the interruption number and the above described data area ID, thus the register bank control unit 8 requests the access right for the data area with respect to the task during execution (STEP S113).

30 When the interruption processing of the interruption number "1"

is attempted to read the data existing in the area "B", the interruption processing of the interruption number "1" does not possess such the access right according to the data area access right definition table shown in Fig. 8 (STEP S 113 / NO).

- 5 Consequently, the memory address space extension device shown in Fig. 7 does not execute the access to the data area "B". Namely, the interruption processing of the interruption number "1" described above becomes the system error (STEP S115).

When the interruption processing of the interruption number "1" is attempted to rewrite the data existing in the area "A", the interruption processing of the interruption number "1" is permitted about the access to the data area "A" according to the data area access right definition table 81 shown in Fig. 8 (STEP S113 / YES). Consequently, the register bank control unit 8 refers to the register bank selection table 12 within the cache 11 shown in Fig. 3. The register bank control unit 8 requests the register bank number of the data area [area "A"] which is attempted to access by the above interruption processing (the interruption processing of the interruption number "1") (STEP S114).

The address operational unit 75 selects a page register 7 from among the above register bank number, and the above register bank address. The address operational unit 75 obtains the extended address from among the page register data stored in the page register 7, and the above described offset address (STEP S116).

Furthermore, a storage unit such as ROM (read only memory) and so forth storing therein a program in a computer system constitutes the memory address space extension device of Fig. 7. Thus the storage unit of the ROM and so forth constitutes a storage medium according to the present invention. The storage medium stores therein the program indicating processing in order to execute operation described in the above respective embodiment.

It is capable of being used an optical disk, a magneto-optical disk, a magnetic recording medium, a semiconductor memory, and so forth as the storage medium.

According to the first operational example described above, the task ID register stores therein the task ID of the task during execution. Consequently, in the case of the interruption processing, value of the task ID register is not changed. For that reason, the interruption processing becomes capable of accessing to the data to which only predetermined certain task accesses.

Namely, according to the above described first operational example, there exists a data to which only prescribed task is permitted to access. It is incapable of preventing that the wrong interruption processing accesses to such the data.

However, according to the above described third operational example, it causes wrong access to be prevented from the task that the access is not permitted with respect to certain data area. Further, it becomes possible to prevent wrong access according to the interruption processing with respect to certain data area. As a result thereof, reliability of the data is improved in the above data area.

(FOURTH OPERATION)

Fig. 8 is view showing the fourth data area access right definition table in the embodiment of the present invention. Hereinafter, there will be described operation of preventing wrong access referring to Figs. 2, 7, and 9. The memory address space extension device shown in Fig. 7 enable the wrong access to be prevented from the task which is not permitted access with respect to certain data area. Also, the memory address space extension device enable wrong access according to the interruption processing to be prevented.

Furthermore, the fourth operational example differs from the third operational example described above. The different point is

processing concerning the access right judgement of either the task during execution or the interruption processing (processing of STEP S113 shown in Fig. 11). Thus, there will be described with respect to this processing.

5 The fourth operational example differs from the third operational example in the data area access right definition table. The data area access right definition table 81 shown in Fig. 8 indicates area to which the access right is permitted in every task ID, or in every interruption number.

10 By contrast, the data area access right definition table 91 shown in Fig. 9 defines the access right with respect to the area that it is capable of executing only write of the data in every task ID, or in every interruption number (In Fig. 9, referred to as "W"). The data area access right definition table defines the access right with respect to the area that it is
15 capable of executing only read of the data (In Fig. 9, referred to as "R"). The data area access right definition table defines the access right with respect to the area that it is capable of executing both of read of the data, and write of the data (In Fig. 9, referred to as "RW").

 According to Fig. 9, the interruption processing of the interruption
20 number "1" (one), in the case of attempting to read the data existing in the data area "B", the access right is not recognized (according to Fig. 9, defined as "×"). Consequently, the memory address extension device shown in Fig. 7, does not execute access with respect to the data area "B", but it causes the operation to be terminated as the system error.

25 According to Fig. 9, the interruption processing of the interruption number "1" (one), in the case of attempting to read the data existing in the data area "A", the access right is recognized (according to Fig. 9, defined as "R"). Consequently, the memory address space extension device shown in Fig. 7 refers to the register bank selection table 12 existing in
30 the cache 11 shown in Fig. 3, before requesting the register bank number

of the data area "A" to which the interruption processing of the above interruption number "1" attempts to access.

Furthermore, the storage unit such as ROM (read only memory) and so forth storing therein the program in the computer system constituting the memory address space extension device of Fig. 7 constitutes the storage medium according to the present invention. The storage medium stores therein the program indicating processing in order to execute operation explained on the respective embodiments described-above.

It is capable of being used an optical disk, a magneto-optical disk, a magnetic recording medium, a semiconductor memory, and so forth as the storage medium.

The fourth operational example is compared with the above third operational example. According to the fourth operational example, it becomes possible to implement more detailed access restriction in every task, or in every interruption processing. As a result thereof, reliability of the data is further improved.

As described above according to the present invention, there is provided the table of defining that the access right is permissible or the access right is in-permissible by the task with respect to certain data area. Thus, it is capable of preventing wrong access from the task with respect to a certain data area. For that reason, it is capable of protecting the data of the area, thus, it is capable of improving the reliability of the data.

Further, according to the present invention, there is provided the table of defining that the access right is permissible or the access right is in-permissible by the task with respect to certain data area or the interruption processing. Thus, it is capable of preventing wrong access from the task with respect to a certain data area and / or the interruption processing. For that reason, it is capable of protecting the data of the area, thus, it is capable of improving the reliability of the data.

Furthermore, in the above described definition table, it causes confusion that the read, and the write with respect to the data area are possible or in-permissible respectively to be defined, thus it is capable of outputting fine-grained control in answer to the inputted CPU data.

5 While preferred embodiments of the invention have been described using specific terms, the description has been for illustrative purposes only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of following claims.

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